Chips to Startup Programme

CAS — IEEE CIRCUITS AND SYSTEMS SOCIETY

tttc

I²CS — Intelligent Integrated Circuits and Systems Research Group

About Workshop

The VLSI Test Workshop offers an in-depth overview of modern design-for-test (DFT) strategies and critical testing practices for today's complex VLSI systems. It covers key topics including scan-based testing, memory testing, and fault modeling, enabling participants to understand techniques for improving testability and achieving higher fault coverage. The workshop includes expert talks from industry professionals, sessions focused on career guidance, and practical hands-on laboratory training using industry standard VLSI Testing tools. In addition, participants benefit from meaningful networking opportunities with researchers and practitioners, making the workshop highly valuable for those aiming to strengthen their expertise in VLSI testing and semiconductor design.

Pre-requisites

Fundamentals of digital design is required. Familiarity with Unix or Linux is desirable but not mandatory. Exposure to RTL design using HDL will be an added advantage. BTech (3rd/4th Year), MTech, PhD scholars, Faculty, Industry professionals are eligible.

Payment Details

Go to SBI Collect Link:
https://www.onlinesbi.sbi/sbicollect/icollecthome.htm
Chose Category → Educational Institutions , Payee → IIIT Kottayam and Payment Category → i2cs Research Lab
After payment, note down the transaction/DU number
Fill the registration form after fee remittance
Registration fee is NOT refundable
Registration form closes once the limit is reached.
Check, if the registration form is open, before payment
Registration Link: https://tinyurl.com/3fsv9yaj

Patrons

Prof. Prasad Krishna
Director, IIIT Kottayam
Dr. M Radhakrishnan
Registrar, IIIT Kottayam
Prof. Ashok S
Professor In-charge, IIIT Kottayam

Organizers

Dr. Kala S, Asst Professor, ECE
Dr. Ananth A, Asst Professor, ECE
Dr. Minu A Pillai, Asst Professor, ECE
Dr. Lakshmi N S, Asst Professor, ECE

Contact Details

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Registration Details

BTech (3rd or 4th Year)/ PG : Rs. 700
BTech - IIITK students : Rs. 500
PhD Scholars/Faculty : Rs. 1500
Industry Professionals : Rs. 2000

- Includes Registration kit, Participation Certificate, Lunch & Refreshment
- Limited seats based on First Come First Serve basis
- Accommodation in student hostels to limited participants, subject to availability, on a paid basis

3-Day Hands-On Workshop

IIIT Kottayam & TTTC India Presents

Workshop on VLSI Test

Jan 30 - Feb 1, 2026

I²CS Research Lab
Department of ECE, IIIT Kottayam
Valavoor P O, Kottayam–686635, Kerala
🌐 i2cs.iiitkottayam.ac.in

Deadline: Jan 20, 2026

Register here:

Indian Institute of Information Technology Kottayam

IEEE COMPUTER SOCIETY
TTTC
Test Technology Technical Community

Resource Persons

Nikhil Sudhakaran
Director of Engineering
Marvell

Dr. Jaidev Shenoy
Senior Staff Manager–
DFT
Marvell

Akash Shimpi
MTS Silicon Design
Engineer
AMD

Abhishek Chaudhary
Principal Member of
Technical Staff
AMD

Dr. Jaynarayan Tudu
Assistant Professor, CSE
IIT Tirupati

Dr. Binod Kumar
Assistant Professor, EE
IIT Jodhpur

About the Institute

Indian Institute of Information Technology, Kottayam is one among the IIITs that have been established as "Institutions of National Importance" by Ministry of Education, Govt. of India under the ambit of IIIT (PPP) Act 2017. The institute offers 4 year B.Tech and B.Tech(Hons) program with specialized courses covering all major research domains of Electronics and Communication Engineering and Computer Science & Engineering. The students are admitted against the JoSAA/CSAB counselling against the JEE main rank list. Institute also offers MTech in CSE and PhD program in CSE, ECE, Humanities and Mathematics.

About Dept of ECE and I²CS Research Lab

Department of ECE offers both BTech and BTech (Hons) degree, with courses covering wide domain of Electronics Circuits, VLSI & Embedded Systems, Signal Processing & Communication Systems, AI and ML. The department also offers PhD program in these domains.

I²CS Research Lab focuses on R&D in the areas of Hardware Accelerators, VLSI Testing, Approximate Computing, FPGA Design, Hardware Security, Analog RF IC Design etc. Research lab is equipped with state-of-the-art EDA tools for IC design under Chips to Startup (C2S) programme of MeitY, Govt of India. Facilities in research lab include EDA Tools from Synopsys, Cadence, Siemens, and AMD Xilinx FPGA, MicroChip SoC, Nvidia Jetson, Robotics kits, Raspberry Pi, Arduino boards and sensors, Renesas kits, Matlab, etc.

Topics and Schedule

DAY 1
09:30 – 10:00 AM : Inauguration and Introduction to ITC/TTTC
10:00 – 11:00 AM : Introduction to Design for Test – 1
11:00 – 11:30 AM : Networking over Tea / Coffee
11:30 – 01:00 PM : Introduction to Design for Test – 2
01:00 – 02:00 PM : Networking over Lunch
02:00 – 03:15 PM : Scan Based Testing
03:15 – 03:45 PM : Networking over Tea / Coffee
03:45 – 05:00 PM : Fault Models
05:00 – 06:00 PM : DFT as a Career

DAY 2
09:30 – 11:00 AM : Scan Compression & Logic BIST
11:00 – 11:30 AM : Networking over Tea / Coffee
11:30 – 01:00 PM : Memory Testing
01:00 – 02:00 PM : Networking over Lunch
02:00 – 03:00 PM : Test Diagnosis
03:00 – 03:30 PM : Networking over Tea / Coffee
03:30 – 04:30 PM : Test Standards
04:30 – 06:00 PM : Lab Session – 1

DAY 3
09:00 – 11:00 AM : Lab Session – 2
11:00 – 11:30 AM : Networking over Tea / Coffee
11:30 – 01:00 PM : Lab Session – 3
01:00 – 02:00 PM : Networking over Lunch
02:00 – 03:30 PM : Open House and Conclusion
03:30 – 03:45 PM : Networking over Tea / Coffee

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